Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5394	(system adj bus) and (local adj bus)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 09:58
L2	0	1 and (buffer$3 adj signal adj line)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 09:59
L3	4	1 and (level adj translation)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:01
L4	163	1 and (logic adj device)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:02
L5	117561	4 (voltage adj level)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:03
L6	12	4 and (voltage adj level)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:07
L7	129	4 and address	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:07
L8	97	7 and buffer$3	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:08
L9	36	8 and (signal adj line)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:12
L10	0	(buffer$3 adj singal adj line) and memory	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:13
L11	8977	memory and (peripheral adj circuit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:14
L12	21	1 and 11	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:21

L14	5917	11 and (address adj signal adl line)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:22
L15	46	14 and (data adj signal adj line)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:29
L16	241	14 and compatible	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:30
L17	79	16 and (memory adj array)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/10/14 10:31